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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,297	04/13/2004	Takayuki Haze	LEPA122745	4560

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

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05/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,297	HAZE, TAKAYUKI	
	Examiner	Art Unit	
	PAMELA E. PERKINS	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *7-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the request for reconsideration on 5 December 2007. Claims 1-9 are pending; claims 7-9 have been withdrawn from consideration.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (KR 1020030072855) in view of Lei (7,008,867) and Beica et al. (2004/0253804).

Lee et al. disclose a method of forming a structure on a flip chip including subjecting a surface of an insulating layer to electroless copper plating to prepare electroless copper plating layer, which is then coated with photosensitive material; exposing to light and developing the photosensitive material to prepare a resist pattern, which is then plated to form a second plating layer that extends to the sidewalls of the hole in the resist pattern; and removing the resist pattern prepared at the second step and the electroless copper plating layer to provide a structure having an electroless copper plated layer juxtaposed/placed on an insulating layer, a pulse plated layer juxtaposed/placed on the electroless copper plated layer, and a second plated laver

juxtaposed/placed on the pulse plated layer, wherein the layers form the sidewalls of the bump pad (constitution).

Lee et al. do not disclose subjecting a pulsing plating layer to electrolytic copper plating using direct current, to prepare a direct current plating layer and the structure are a bump pad.

Lei discloses a method of forming a bump pad of a flip chip including a subjecting a surface of an insulating layer (10) to electro-chemical copper plating to prepare a copper plating layer (16B) (col. 3, lines 42-62), which is then coated with photosensitive material; exposing to light and developing the photosensitive material to prepare a resist pattern (20) (col. 4, lines 3-10), which is then pulse plated to form a pulse plating layer (22); and subjecting the pulse plating layer (22) to electrolytic copper plating using direct current, to prepare a direct current plating layer (col. 4, line 11 thru col. 5, line 13).

Since Lee et al. and Lei are both from the same field of endeavor, a method of forming a bump, the purpose disclosed by Lei would have been recognized in the pertinent art of Lee et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lee et al. by subjecting a pulsing plating layer to electrolytic copper plating using direct current, to prepare a direct current plating layer as taught by Lei to improve the structural stability of the deposited copper (col. 4, lines 58-64).

Beica et al. disclose a method of forming a structure on a flip chip including forming over an insulating layer (100) a copper plating layer (106), which is then coated with photosensitive material; exposing to light and developing the photosensitive

material to prepare a resist pattern (108), which is then plated to form a second plating layer (112) that extends to the sidewalls of the hole in the resist pattern using a direct current pulse plating process; and removing the resist pattern (108) and the copper plating layer (106) to provide a bump pad (112) having an electroless copper plated layer juxtaposed/placed on the insulating layer (100) (Fig. 1; para. 59-66).

Since Lee et al. and Beica et al. are both from the same field of endeavor, a method of forming a structure on a flip chip, the purpose disclosed by Beica et al. would have been recognized in the pertinent art of Lee et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lee et al. by forming a second plating layer that extends to the sidewalls of the hole in the resist pattern using a direct current pulse plating process; and removing the resist pattern and the copper plating layer to provide a bump pad as taught by Beica et al. to ensure sufficient volume of bump material is provided for the bump pad (para. 64).

Referring to claim 2, Lee et al. disclose the formation the electroless copper plating layer by subjecting the surface the insulating layer to electroless copper plating, and the coating of the photosensitive material on the electroless copper plating layer (constitution).

Referring to claim 4, Lee et al. disclose the photosensitive material coated electroless copper plating layer is a dry film (constitution).

Referring to claim 5, Lei disclose wherein the second step comprises formation of the resist pattern through exposure light and development of the photosensitive

material, and the formation of the pulse plating layer by subjecting resist pattern electrolytic pulse plating (col. 4, lines 33-57).

Referring to claims 3 and 6, Lee et al. disclose the photosensitive layer and plating layer of claim 1. It would have been obvious to one having ordinary skill in the art at the time invention was made to form the photosensitive layer as 20 μm thick and the pulse plating layer as 5-10 μm thick disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

Applicant's arguments filed 5 December 2007 have been fully considered but they are not persuasive. As stated above, Lee in view of Lei and Beica et al. discloses the method of forming a bump pad of a flip chip as described in claims 1-6.

In response to the applicant's arguments, the applicant argues Lei does not disclose pulse plating over the electroless copper layer or subjecting the pulse plating layer to electrolytic copper plating using a direct current. However, Lee in combination with Lei teach subjecting a surface of an insulating layer to electroless copper plating to prepare electroless copper plating layer (Lee: constitution), which is then pulse plated to form a pulse plating layer; and subjecting the pulse plating layer to electrolytic copper plating using direct current preparing a direct current plating layer (Lei: col. 5, lines 1-13) to improve the structural stability of the deposited copper (Lei: col. 4, lines 58-64).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAMELA E. PERKINS whose telephone number is (571)272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

PEP
12 May 2008